CLAIMS

What is claimed is:

1. A method for forming an alignment mark structure (148) for a semiconductor device, the method comprising:

forming an alignment recess (130) at a selected level of the semiconductor device substrate;

forming a first metal layer (140) over said selected substrate level and within said alignment recess (130), wherein said alignment recess (130) is formed at a depth such that said first metal layer (140) only partially fills said alignment recess (130);

forming a second metal layer (142) over said first metal layer (140) such that said alignment recess (130) is completely filled;

planrizing said second metal layer (142) and said first metal layer (140) down to said selected substrate level, thereby creating a sacrificial plug (144) of said second layer material within said alignment recess; and

removing said sacrificial plug (144) in a manner so as not to substantially roughen the planarized surface at said selected substrate level.

2. The method of claim 1, wherein said second metal layer (142) has an etch selectivity with respect to said first metal layer (140).

3. The method of claim 3, wherein said second metal layer (142) further has an etch selectivity with respect to a dielectric material surrounding said alignment recess (130).

4. The method of claim 2, wherein:

said first metal layer (140) comprises tantalum nitride; and

second metal layer (142) is a sacrificial bilayer of tantalum and copper.

5. The method of claim 2, further comprising depositing an adhesion layer for adhering said second metal layer (142) to said first metal layer (140).

6. The method of claim 2, wherein said second metal layer (142) is deposited by one of: physical vapor deposition (PVD), chemical vapor deposition (CVD), and plating.

7. The method of claim 2, wherein said sacrificial plug (144) is removed with a dilute phosphoric acid etch.

8. The method of claim 1, wherein the semiconductor device comprises a magnetic random access memory (MRAM).

9. The method of claim 8, wherein the MRAM is a field effect transistor (FET) based MRAM device (102).

10. The method of claim 8, wherein said alignment recess (130) is formed at a greater depth than a depth of a via (116) used to connect a metal strap (112) of the MRAM device to a lower metallization level line (114) of the MRAM device.

11. The method of claim 10, wherein:

said selected level of the device is a level at which said metal strap (112) is defined; and

the material used to form said metal strap (112) is metallic and opaque.

12. The method of claim 10, wherein said alignment recess (130) is defined simultaneously with said via (116), and said alignment recess (130) is fully formed by an overetch.

13. The method of claim 9, wherein said alignment recess (130) is defined subsequent to the formation of said via (116).